Insulating Gate III-N Heterostructure Field-Effect Transistors for High-Power Microwave and Switching Applications

M. Asif Khan, *Senior Member, IEEE*, Grigory Simin, *Member, IEEE*, Jinwei Yang, Jianping Zhang, Alexei Koudymov, Michael S. Shur, *Fellow, IEEE*, Remis Gaska, Xuhong Hu, *Member, IEEE*, and Ahmad Tarakji

***Abstract*—We describe the properties of novel III-N-based insulating gate heterostructure field-effect transistors (HFETs). For the gate isolation, these devices use either SiO_2 layer (in metal–oxide–semiconductor HFET (MOSHFET) structures) or Si_3N_4 layer (in metal–insulator–semiconductor HFET structures). These insulating gate HFETs have the gate-leakage currents 4–6 orders of magnitude lower than HFETs, even at elevated temperatures up to 300 °C. A double-heterostructure MOSHFET with SiO_2 gate isolation exhibits current collapse-free performance with extremely low gate-leakage current. Insulating gate devices, including large periphery multigate structures, demonstrate high-power stable operation and might find applications in high-performance power amplifiers and microwave and high-power switches with operating temperatures up to 300 °C or even higher.**

***Index Terms*—AlGaN, FET, GaN, heterostructure FET (HFET), microwave, metal–oxide–semiconductor HFET (MOSHFET).**

I. Introduction

UNIQUE materials properties of GaN-based semiconductors stimulated a great deal of interest in research and development in materials growth and opto-electronic and electronic devices using this semiconductor system. The major advantages of nitride-based devices that make them extremely promising for high-power high-temperature applications are high electron mobility and saturation velocity, high sheet carrier concentration at heterojunction interfaces, high breakdown field, and low thermal impedance (when grown over SiC or bulk AlN substrates). The chemical inertness of nitrides is another key property. An AlGaN/GaN heterostructure field-effect transistor (HFET) is one of the most promising electronic devices, which has been a topic of intensive investigations since the first report in 1991 [1], [2]. Several groups demonstrated high-power operation of AlGaN/GaN HFETs at microwave frequencies [3]–[5], including a 100-W output-power single-chip amplifier developed by Cree Inc., Durham, NC, and devices with 100-GHz cutoff frequency reported in [6]. The characteristics of III-N HFETs can be further improved by implementing a new approach, which results from the demonstration of good quality of SiO_2/AlGaN and Si_3N_4/AlGaN interfaces. This approach opens up a way to fabricate insulated gate field-effect transistors (FETs), which have the gate-leakage currents several orders of magnitude below those of regular HFETs, and exhibit better linearity and higher channel saturation currents. In this paper, we describe design, characterization, and applications of these new devices.

Manuscript received April 2, 2002. The work of M. A. Khan, G. Simin, J. Yang, J. Zhang, and A. Koudymov was supported in part by the Ballistic Missile Defense Organization under Army Space and Missile Defense Command (SMDC) Contract DASG60-98-1-0004, monitored by T. Bauer, B. Strickland, and K. Wu and under Army SMDC Contract DASG60-00-10003, monitored by T. Bauer. The work of M. S. Shur was supported by the Office of Naval Research under Compact Multiuniversity Research Initiative, monitored by J. Zolper and H. Dietrich. The work of R. Gaska, X. Hu, and A. Tarakji was supported by the Missile Defense Agency under Small Business Innovative Research (SBIR) Contract F33615-01-C-1911, monitored by G. Gillispie of Wright-Patterson Air Force Base, and under Army SMDC Contract DASG60-00-C-0088, monitored by F. Clark.

M. A. Khan, G. Simin, J. Yang, J. Zhang, and A. Koudymov are with the Department of Electrical Engineering, University of South Carolina, Columbia, SC 29208 USA.

M. S. Shur is with the Electrical, Computer, and Systems Engineering, Department, Rensselaer Polytechnic Institute, Troy, NY 12180 USA.

R. Gaska, X. Hu, and A. Tarakji are with Sensor Electronic Technology Inc., Columbia, SC 29209 USA.

Digital Object Identifier 10.1109/TMTT.2002.807681

II. Metal–Oxide–Semiconductor Heterostructure Field-Effect Transistor (MOSHFET) Fabrication and Characteristics

Recently, we demonstrated novel AlGaN/GaN MOSHFETs on sapphire [7] and SiC [8] substrates. The MOSHFET design combines the advantages of the MOS structure, which suppresses the gate-leakage current, and an AlGaN/GaN heterointerface that provides high-density high-mobility two-dimensional (2-D) electron gas channel. The MOSHFET approach also allows for application of high positive gate voltages to further increase the sheet electron density in the 2-D channel and, therefore, the peak device current. The MOSHFET built-in channel is formed by the high-density 2-D electron gas at the AlGaN/GaN interface as in regular AlGaN/GaN HFETs. However, in contrast to a regular HFET, the gate metal is isolated from the AlGaN barrier layer by a thin SiO_2 film [see Fig. 1(a)]. Thus, the MOSHFET gate behaves more like a MOS gate structure rather than a Schottky barrier gate used in regular HFETs. Since the properly designed AlGaN barrier layer is fully depleted by electron transfer to the adjacent GaN layer, the gate insulator in the MOSHFET consists of two sequential layers: the SiO_2 film and AlGaN epilayer. This double layer ensures an extremely low gate-leakage current and allows for a large negative to positive gate voltage swing. Due to the wide bandgap and to the full depletion of the AlGaN barrier, neither electron, nor hole parasitic channel forms at the SiO_2–AlGaN interface at the gate voltages up to $+10$ V.

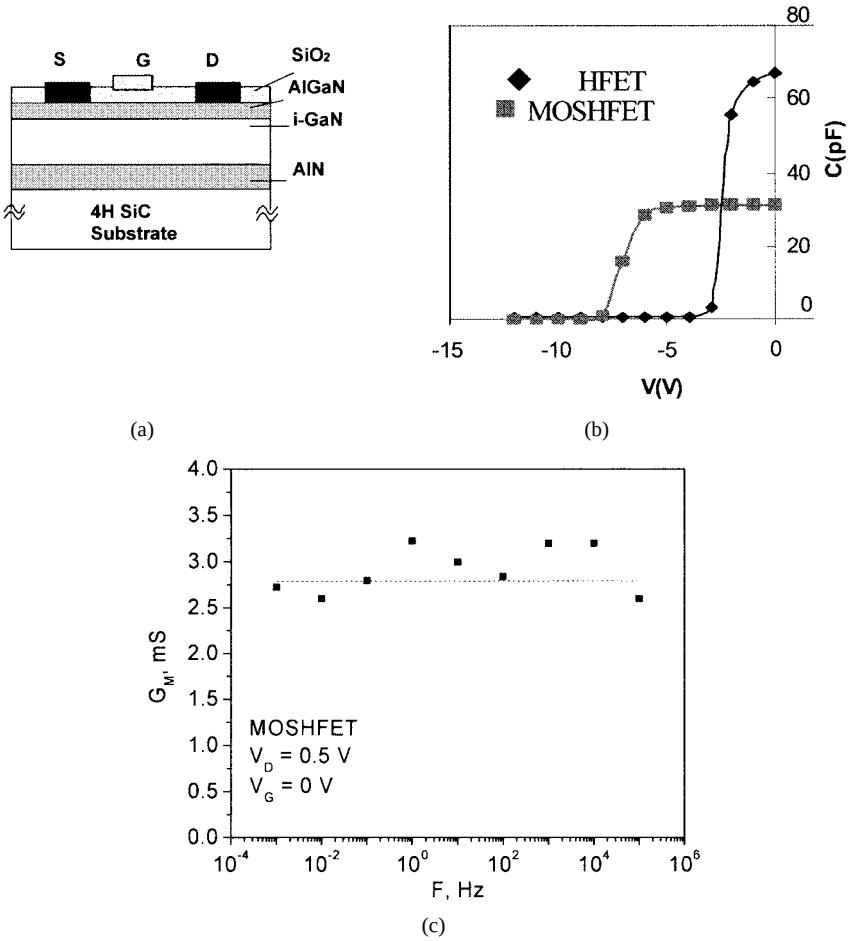


Fig. 1. (a) Schematic MOSHFET layout. (b) Capacitance–voltage characteristics of MOSHFET and HFET test structures. (c) Small-signal transconductance dispersion of the MOSHFET.

The device epilayer structures were grown by low-pressure metal organic chemical vapor deposition (LP-MOCVD) on insulating 4H–SiC substrates. The AlGaN/GaN layers for this structure were deposited at 1000 °C and 76 torr. A 50-nm AlN buffer layer was first grown at 1000 °C, followed by the deposition of a 1.5-μm insulating GaN layer. The heterostructure was capped with a 30-nm $Al_{0.2}Ga_{0.8}N$ barrier layer, which was unintentionally doped. We also had a low-level flux of trimethylindium (TMI) present during the growth of all the layers of the structure. We had a low-level flux of TMI present during the growth of all the layers of the structure. Also, small concentration of carbon was present in all our grown layers. The presence of the indium (In) surfactant and of trace amounts of In helps in improving the surface and interface roughness. As shown in [9], the surface roughness decreases from 7-nm rms to 2.5-nm rms with incorporation of In. The beneficial role of carbon was explained in [10]. We found the combination of In and carbon in all our layers to be especially beneficial for both improving the materials quality and for obtaining better ohmic contacts. The measured room-temperature Hall mobility and sheet carrier concentration were 1200 $cm^2/V \cdot s$ and 1.2×10^{13} cm^{-2}, respectively.

Transistor devices were fabricated using Ti(200 Å)/Al(500 Å)/Ti(200 Å)/Au(1500 Å) for the source–drain ohmic contacts. These were annealed at 850 °C for 1 min in nitrogen ambient. A reactive ion etching (RIE) was used for device isolation. Prior to the gate fabrication, a 10-nm SiO_2 layer was deposited on part of the heterostructure using plasma-enhanced chemical vapor deposition. The thickness of this layer ($d_{\rm OX}$) was extracted from the capacitance–voltage (C–V) measurement at 1 MHz on the regions with and without the SiO_2 layer. In Fig. 1(b), we include the C–V plots for 100 μm $\times$ 200 μm pads over the HFET and MOSHFET regions. From the 0-V capacitance of these metal–semiconductor structures (without an SiO_2 layer), and using AlGaN layer permittivity $\varepsilon_B = 8.8$, we estimate the AlGaN barrier thickness d_B to be 23 nm. This is very close to the 25-nm value estimated from the deposition rate.

The oxide thickness $d_{\rm OX}$ can be extracted from the measured pad capacitances

$$C_{\rm MOS} = \frac{\varepsilon_0 \varepsilon_B}{d_B} \times \left(1 + \frac{d_{\rm OX}}{d_B} \cdot \frac{\varepsilon_B}{\varepsilon_{\rm OX}}\right)^{-1} = C_{MS} \times \left(1 + \frac{d_{\rm OX}}{d_B} \cdot \frac{\varepsilon_B}{\varepsilon_{\rm OX}}\right)^{-1}. \quad (1)$$

Here, $C_{\rm MOS}$ and C_{MS} are the capacitances of equal area pads on the oxide and nonoxide areas and $\varepsilon_{\rm OX} = 3.9$ is the SiO_2 dielectric permittivity. Using the data of Fig. 1 and (1), the SiO_2

thickness $d_{\rm OX}$ was estimated to be 11 nm. This value is in reasonable agreement with the $d_{\rm OX}$ value of 10 nm expected from the deposition rate. Due to a larger gate-to-channel separation, the threshold voltage of the MOSHFET is larger than that of the HFET. Assuming the same sheet charge density in the channel for MOSHFET and HFET devices at zero gate bias and ignoring the surface charge at the SiO_2/AlGaN interface, the threshold voltages for the MOSHFET and HFET can be related as

$$Q_S = qN_S = C_{\rm MOS} \times V_{\rm TMOS} = C_{MS} \times V_{TMS} \tag{2}$$

or

$$V_{\rm TMOS} = V_{TMS} C_{MS}/C_{\rm MOS} = V_{TMS} \times \left(1 + \frac{d_{\rm OX}}{d_B} \cdot \frac{\varepsilon_B}{\varepsilon_{\rm OX}}\right). \tag{3}$$

For the MOSHFET data of Fig. 1, the threshold voltage increases 2.1 times compared to the HFET. The threshold voltages of the MOSHFET (~7.5 V) and HFET (~3.5 V) extracted from the C–V characteristics of Fig. 1 are in good agreement with the above estimate. The deviation of the measured data from the estimate given by (3) is related to the interface charge. Since this deviation is small, the surface charge density at the SiO_2/AlGaN interface must be sufficiently low compared to qN_s at zero gate bias. To further prove the absence of significant surface trapping, we have measured the frequency dependence of the small-signal transconductance in the linear regime at low drain voltage and zero gate bias. Zero gate bias was chosen to eliminate the effects related to the current collapse (see below). The measurements were done on a number of MOSHFETs from different wafers. For comparison, we have also measured HFET devices fabricated on the same wafers. No difference between HFET and MOSHFET behavior was observed. Fig. 1(c) shows typical frequency dependence of small-signal transconductance for the MOSHFET device. As seen, the MOSHFET does not exhibit any noticeable dispersion. The predicted and measured increase in the threshold voltage is not detrimental for high-power high-voltage nitride-based devices. The MOSHFET transconductance is approximately 50% lower compared to HFET due to larger gate–channel separation. However, the linearity of the transconductance–gate voltage dependence for the MOSHFET is much better compared to that for the HFET. Therefore, as shown below, the MOSHFET has lower nonlinear distortions in high-power microwave and switching applications.

The suppression of the gate-leakage current is one of the most important features of the MOSHFET. In Fig. 2, we show the gate-leakage current for the 1.5 μm × 200 μm gate MOSHFET at different temperatures. The data shows that the MOSHFET leakage current is as low as 200 pA at −20-V gate bias at room temperature and is approximately six orders of magnitude smaller than for the regular HFET with similar gate dimensions, which is presented for reference in the Fig. 2. Even at +300 °C, the gate-leakage current for MOSHFET remains 3–4 orders of magnitude lower than for regular HFETs. The pinchoff characteristics of the AlGaN/GaN MOSHFET were also measured in the temperature range of 25 °C–300 °C. The pinchoff current as low as 0.15 nA/mm at room temperature and 38 μA/mm at 250 °C was measured at the gate voltage $V_g = -15$ V and the drain bias of 10 V.

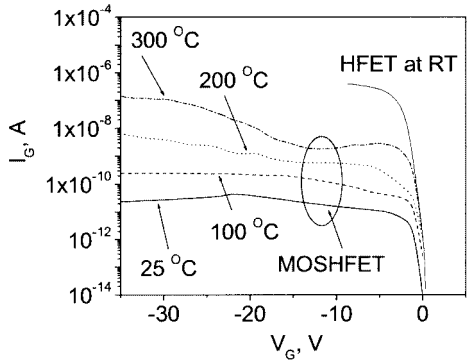


Fig. 2. Gate-leakage currents for the MOSHFET at different temperatures and the baseline HFET at room temperature measured in diode mode (drain disconnected).

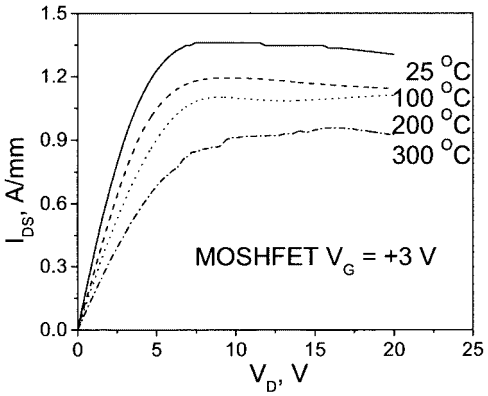


Fig. 3. I–V characteristics of a MOSHFET with the source–drain opening of 5-μm and gate length of 1.5 μm.

Fig. 3 shows the measured current–voltage (I–V) characteristics of an AlGaN/GaN MOSHFET with a source–drain separation of 5 μm and a gate length of 1.5 μm at elevated temperatures at the gate bias $V_{\rm G} = +3$ V. As seen, the device saturation current is close to 1 A/mm. This current decrease with the temperature follows the temperature dependence of the electron saturation velocity [11].

The maximum dc saturation drain current $I_{\rm DSM}$ at positive gate voltages is a key parameter controlling maximum output RF power. For conventional AlGaN/GaN HFETs, gate voltages in excess of +1.2 V result in excessive leakage current, which limits $I_{\rm DSM}$. In a MOSHFET, the gate voltages as high as +10 V could be applied. This results in an approximately 100% increase in the $I_{\rm DS}$ value with respect to the zero gate-bias value. The gate leakage, however, remains well below 1 nA/mm. Fig. 4 shows the transfer characteristics for the 1-μm gate MOSHFET and HFET measured at the drain voltage sufficient to shift the operating point into the saturation regime. Fig. 4 also shows the gate-bias dependence of the HFET and MOSHFET current in the saturation regime (for the MOSHFET, the gate current remains in the low nanoampere range). As seen, the gate voltage corresponding to the maximum of $I_{\rm DS}$ in the HFETs also corresponds to a sharp increase of the gate-leakage current. This indicates that the mechanism responsible for the $I_{\rm DS}$ saturation at high gate bias is the gate-leakage current. This explains why the measured values of $I_{\rm DSM}$ for the HFETs at high gate

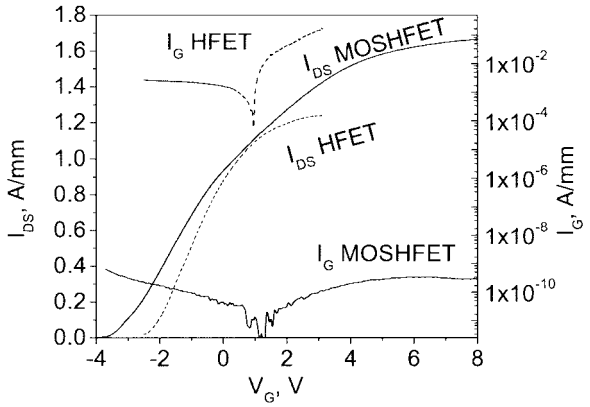
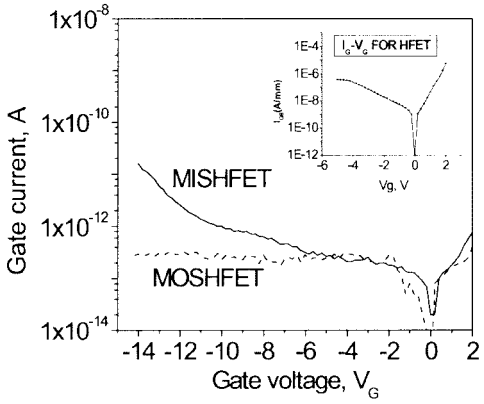


Fig. 4. Maximum saturation and gate-leakage currents in 1.5-μm gate MOSHFET and HFET devices.

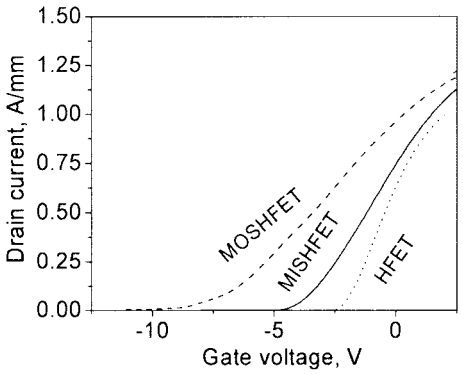
bias are substantially smaller than those predicted by the approximation based on the 2-D electron channel capacity [12]. In the MOSHFETs, where the gate leakage is suppressed, the 2-D electrons spillover into the AlGaN barrier becomes a limiting mechanism. According to the model developed in [13], this electron spillover occurs at the source edge of the gate at a certain value of the gate voltage (V_{GM}) that depends on the geometry of the 2-D channel and on the Fermi-level position. A larger gate–channel separation in the MOSHFET also contributes to a higher value of V_{GM} for MOSHFETs. Due to these factors, both the MOSHFET saturation gate voltage and the saturation current for the MOSHFETs are higher than those for the HFETs. Assuming that the maximum sheet carrier density in the 2-D electron gas (2-DEG) channel (limited by the 2-D density of states) n_s is approximately 2×10^{13} cm^{-2} [14] and the effective electron drift velocity in the channel $v = 5 \times 10^6$ cm/s, we estimate the maximum achievable channel current $I_{\rm DSM}/{\rm W} = q \times n_s \times v \approx 1.6$ A/mm. The measured saturation current in our MOSHFET is close to this maximum value.

III. Si_3N_4-Based Insulating Gate Devices: Metal–Insulator–Semiconductor HFETs (MISHFETs)

The SiO_2 material is not the only choice for making insulating gate III-N devices. In the past, the MOSFETs using Ga_2O_3/Gd_2O_3 as the gate insulator [15] were reported. However, the charge control in this structure was fairly poor and the transconductance achieved was not high enough for practical applications. The use of Si_3N_4 for insulating gate III-N devices was first proposed in [16]. Several groups have recently shown that Si_3N_4 passivation in the source–gate and gate–drain region improves the device performance and reduces the transconductance dispersion [17], [18]. These results suggest that the high quality of the insulator/barrier interface can also be achieved using Si_3N_4 material. We have fabricated insulating gate transistors using Si_3N_4 [19]. We called these devices MISHFETs. A device fabrication procedure was similar to that reported earlier for the MOSHFETs. Two sets of devices with identical geometry (gate length 1 μm, source–drain opening 5 μm, and gatewidth 100 μm) were fabricated on the same wafer. They consisted of MOSHFETs (100-Å SiO_2 under the gate and in the source–gate and drain–gate regions) and MISHFETs (100-Å Si_3N_4 insulator replacing SiO_2). Both the SiO_2 and the Si_3N_4 layers were deposited using plasma-enhanced chemical vapor deposition (PECVD). In Fig. 5(a) and (b), we include the transfer curves and gate-leakage current curves, respectively, for the MOSHFETs and MISHFETs. As seen, the maximum saturation currents in both the MOSHFET and MISHFET are close. Either oxide or the nitride insulator layers reduce the gate leakage from six to five orders correspondingly below that measured for the typical HFET devices. The gate-leakage current of the MISHFET is higher than of the MOSHFET, probably due to a lower quality of the thin Si_3N_4 layer. However, the increase in the threshold voltage for the MISHFET device is not as large. This follows directly from a higher value of the dielectric constant of the Si_3N_4 layer ($\varepsilon_R = 3.9$ for SiO_2 and $\varepsilon_R = 7.5$ for Si_3N_4).



(a)



(b)

Fig. 5. (a) Gate-leakage current and (b) transfer characteristics comparison for the MOSHFET and MISHFET fabricated on the same wafer (after [16]). The inset shows the gate-leakage current for a regular HFET.

IV. RF-Current Collapse in MOSHFETs and MISHFETs

A so-called current collapse [20]–[23] and long-term stability are the most important problems preventing large-scale practical usage of nitride-based HFETs in ultra-high power microwave systems. The current collapse manifests itself as a reduction of the device current when a large RF signal is applied to the gate. This reduction is the main reason why the output power of AlGaN/GaN HFETs is considerably smaller than the value expected based on steady-state I–V characteristics. For example,

a typical AlGaN/GaN HFET with the maximum saturation current about $I_{\rm DSM} \approx 1$ A/mm and the knee voltage $V_{\rm KN} \approx 5$ V at a moderate operating point of $V_D = 35$ V should deliver an output power

$$P_{\rm OUT} \approx I_0 \times (V_D - V_{\rm KN})/2 \approx 7.5 \text{ W/mm} \qquad (4)$$

where $I_0 \approx I_{\rm DSM}/2$ is the operating dc current. However, for such a device, even under pulsed drain bias and pulsed RF drive conditions eliminating the device self-heating, the measured RF output power is typically approximately 2–4 W/mm (excluding some hero device results, which show the power close to this expected value or higher, usually for a short time).

The maximum output power depends strongly on the input–output impedance matching. As we recently showed [20], a precise source– and load–pull tuning leads to the measured values of the output power that are very close to those given by (4) if, instead of I_0, one uses the actual value I_{00} of the device dc current measured under an RF drive on the gate. Hence, we conclude that the impedance mismatch is not the main reason for the difference between the expected and measured RF powers. We have also shown in [20] that I_{00} reduces from I_0 much more than might be expected from transistor transfer curve nonlinearity or self-biasing, and that this difference is a direct manifestation of the current collapse.

The collapse phenomenon has been observed in almost all AlGaN/GaN HFETs and MOSHFETs. However, in spite of a large number of studies of the current collapse (see [21]–[26]), the physical mechanism of the effect has remained somewhat mysterious. In this paper, we present the results of the experiments that allow us to identify the device active layer regions responsible for the current collapse and compare the current collapse in the MOSHFET, MISHFET, and HFET devices. In order to compare the current collapse effects in MISHFET, MOSHFET, and HFET devices, we measured their pulsed I–V characteristics (see Fig. 6). For these measurements, the source–drain bias was fixed at a value well in the saturation regime. The gate voltage was then pulsed using 1-μs pulses with a 50% duty cycle. The gate–voltage pulse amplitude varied from 0 V (channel open) to a value below the devices threshold voltage. The "return" pulsed current, i.e., the pulsed current when the gate voltage pulse returns to zero [as shown in Fig. 6(a)] was measured. Since the three device types had different threshold voltages, we plotted in Fig. 6 the gate voltage normalized to the threshold voltage and the pulse current normalized to the dc current at zero gate bias. As seen, at a nonzero value of the gate bias pulse, the device current does not return to its dc value ($I_{\rm DC}$) for the gate pulse voltage ($V_{\rm G} = 0$). This is the manifestation of the current collapse. After a negative voltage is applied to the gate, it takes a certain amount of time for the current to recover to its peak value when the gate voltage returns back to $V_{\rm G} = 0$. Therefore, the difference between dc and pulsed values of drain currents at zero gate voltage (illustrated by the arrowhead line) is a direct measure of the RF-current collapse. As seen, this reduction in current is present for all measured devices. The presence of the SiO_2 layer practically does not affect the current collapse. However, the current collapse in the Si_3N_4MISHFET occurs at the gate voltage amplitude larger than those for MOSHFET and HFET

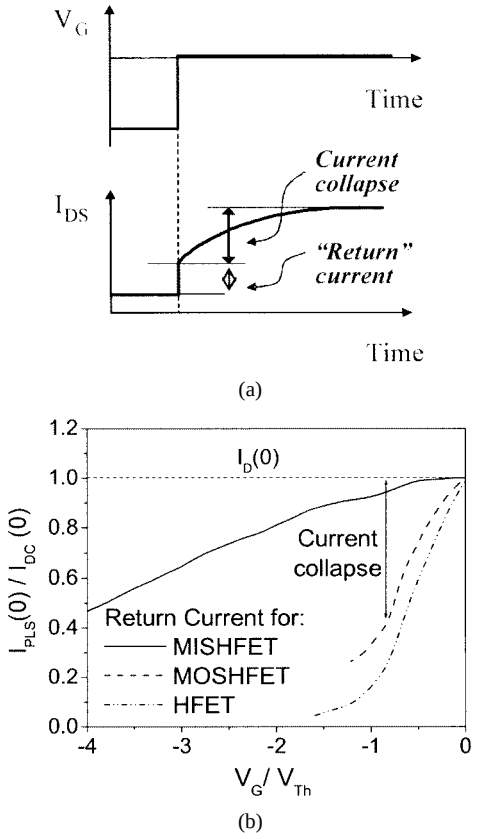


Fig. 6. Pulsed measurements of the current collapse in III-N HFETs (after [16]). The pulsewidth is 1 μs, duty cycle 50%. The return current was measured immediately (within $\sim$20 ns) after gate pulse removal.

devices, i.e., the MISHFETs exhibit lesser RF current collapse. Several mechanisms might be responsible for this difference. Surface charge modification at SiO_2/AlGaN or Si_3N_4/AlGaN interfaces may be different. It is also possible that the Si_3N_4 being extremely hard material reduces the deformation of the HFET cap/channel layer caused by strong electric field under the gate (this possible mechanism was proposed in [27]).

We used gated transmission line model (GTLM) measurements [27], [28] on HFET and MOSHFET devices under pulsed gate-bias conditions in order to isolate the changes of channel resistance under the gate and outside the gate during the transient. The gate lengths in sequential sections of the GTLM varied from $L_{\rm G} = 10$ μm to $L_{\rm G} = 100$ μm, whereas the gate–source and gate–drain openings were kept constant at $L_{\rm GS} = L_{\rm GD} = 10$ μm. The width of all the sections was $W = 200$ μm. Gate voltage pulses (typically 1–100-s long) were used to bias the devices from pinchoff to the zero gate-bias conditions. The total resistances of the GTLM sections $R_T(0)$ and $R_T(\tau)$ were measured in the beginning of the transient process ($t = 0$) and at the end of the gate pulse ($t = \tau$, when the current is close to its steady-state value), respectively. The dependences $R(L_{\rm G})$ in both linear mode ($V_{\rm DS}$ is less than the knee voltage) and saturation mode (high $V_{\rm DS}$) are straight lines with the slopes being inversely proportional to the channel resistance *under the gate* with the intercept at $L_{\rm G} = 0$ giving the total resistance *outside the gate*. Our measurements [27] showed that the current collapse under pulsed gate bias results from the edge effects at the source and/or drain sides of the

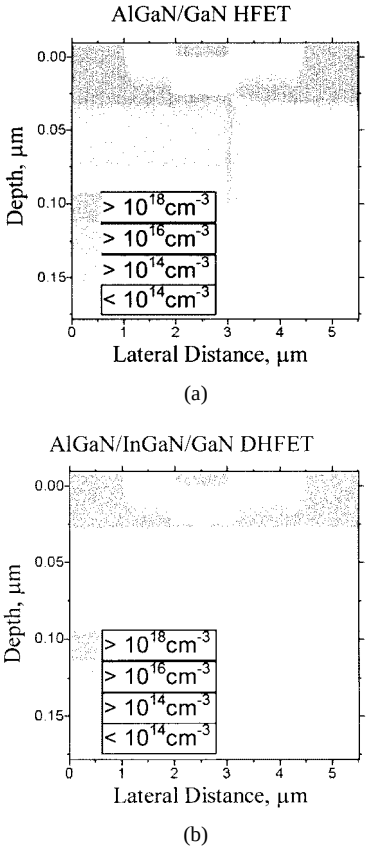


Fig. 7. Simulated 2-DEG density distribution in conventional: (a) HFET and (b) DHFET structures. The simulations were performed at +30 drain voltage and −2-V gate bias.

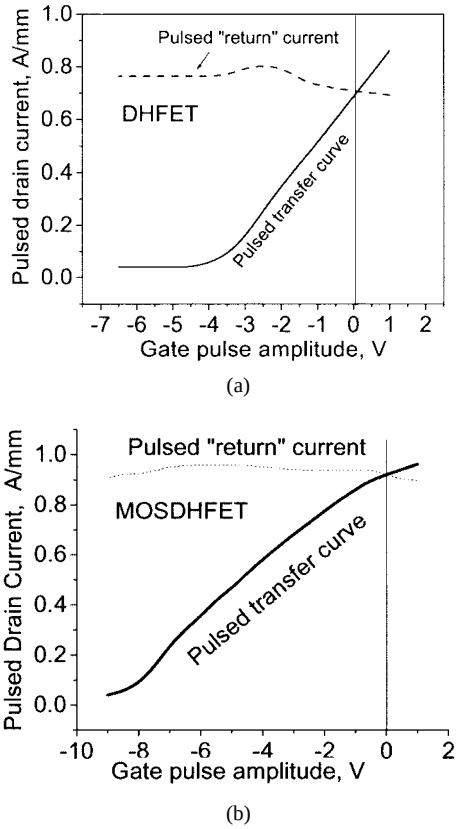


Fig. 8. Pulsed I–V characteristics of: (a) DHFET and (b) MOSDHFET. Dashed lines show the pulsed current measured when the gate pulse voltage returns to zero value (pulsed "return" current). Compare to Fig. 6.

gate. These effects may include the charge trapping in the AlGaN barrier and in the GaN buffer, as well as surface charge modulation. As we will see from the following discussion of our double heterostructure design below, the charge trapping due to electron spillover into AlGaN and, possibly, GaN layers seems to be the most important mechanism responsible for the current collapse. No difference between the HFET and MOSHFET behavior was observed.

V. Insulating Gate Double-Heterostructure Field-Effect Transistors (DHFETs)

The MOSHFET and HFET devices fabricated from the same wafer exhibit nearly the same degree of current collapse. In other words, SiO_2 layer incorporation under the gate does not affect the mechanism responsible for the current collapse in AlGaN/GaN HFETs. The presence of the Si_3N_4 layer does not eliminate the current collapse completely as well. We recently proposed and demonstrated a DHFET where the 2-DEG channel is confined within a thin InGaN layer sandwiched between the GaN buffer and AlGaN barrier [29]. The insertion of the InGaN layer forms a quantum well with the depth and shape being determined by AlGaN/InGaN and GaN/InGaN bandgap offsets and interface polarization charges. This quantum well significantly improves the confinement of the channel electrons for all applied drain- and gate-bias voltages. The electron spatial distributions in a regular HFET and DHFET structures are shown in Fig. 7. A significantly reduced electron spillover is clearly seen in the DHFET as compared to the HFET structure. This should significantly reduce the total charge that can be trapped outside the channel. This practically eliminates the current collapse. This was confirmed by pulsed measurements similar to those discussed above for the MOSHFET, MISHFET, and HFET. This data for DHFET and MOSDHFET are shown in Fig. 8. As seen, the pulse return current for these devices is nearly independent on the gate amplitude and is very close to the dc current at zero gate bias.

We also fabricated a novel structure combining the advantages of the SiO_2 gate insulation (MOSHFET) and the InGaN channel DHFET design [30]. The resulting metal–oxide–semiconductor double heterostructure FET (MOSDHFET) devices are current collapse free and exhibit gate-leakage currents approximately 4–6 orders of magnitude lower than the regular Schottky gate HFETs (depending on the thickness and quality of the oxide layer). As described in Section I, the epilayers for the MOSDHFET were grown on insulating SiC substrates using conventional LP-MOCVD. The growth temperatures for the GaN buffer, InGaN channel, and AlGaN barrier layers were 1000 °C, 760 °C, and 1100 °C, respectively. The InGaN were doped n-type with their bulk electron concentration of approximately 2×10^{17} cm^{-3}. The presence of In the InGaN layer was confirmed by secondary ion mass spectrometry (SIMS) profiling. The room-temperature Hall mobility and the sheet carrier concentration for the deposited DHFET structure were measured to be 730 cm^2/V · s and 1.1×10^{13} cm^{-3}, respectively. The MOSDHFET device fabrication procedure is similar to that used earlier for the MOSHFETs. Devices with

a 5-μm source–drain opening and a 1-μm gate length were fabricated. Several DHFET devices were also fabricated on the same wafer by protecting the source–drain opening during SiO_2 deposition. As reported earlier for the MOSHFET devices, the threshold voltage of MOSDHFETs is larger than that for the HFETs. The DHFET and MOSDHFET threshold voltages ($V_T \approx -4.8$ V and $V_T \approx -10$ V, respectively) calculated using (2) and (3) correspond closely to our experimental data. The gate-leakage current for the MOSDHFET device was below 10 pA for gate voltages $V_G = 0, \ldots, -15$ V. In the DHFET, the gate-leakage current for the same gate voltage range increased up to 10 μA. Therefore, as we could see for the MOSHFET devices before, the introduction of the thin SiO_2 layer decreases the gate-leakage current of the DHFET by approximately 4–6 orders of magnitude. The pulse MOSDHFET characteristics show the return current that is very close to the dc value at zero gate bias, therefore, not exhibiting any current collapse. As shown below, the MOSDHFET devices also demonstrate stable current collapse-free behavior under intense RF drive conditions.

VI. Multigate Large-Periphery MOSHFETs and MOSDHFETs

In this section, we describe large periphery multigate (MG) MOSHFET and MOSDHFET devices, fabricated on SiC substrates, using oxide bridging for source interconnects [31]. These high-power devices demonstrate a nearly linear dependence of saturation current, transconductance, microwave gain, and saturation power on the total device width in the range from 0.15 to 4 mm. The MG device geometry consists of an interlaced source–gate–drain electrode structure. The source-to-source connections go over the gate electrodes with an oxide layer in between used for isolation. This MG MOSDHFET design is shown in Fig. 9. Unlike for single-section dual-gate MOSDHFET processing, we use PECVD to deposit 0.3-μm-thick SiO_2 isolation "islands" at the gate–source intersections for the MG device. Ti(200)/Au(6000) metal electrodes are then deposited to form low-resistance section interconnects and device contact pads. A relatively low dielectric permittivity of the SiO_2 islands allows for the bridging with a small parasitic capacitance. For the 5 μm $\times$ 5 μm source–gate overlap area and 0.3-μm-thick islands, the bridge capacitance is only 0.003 pF. This is approximately 100 times lower than the gate capacitance of a MOSHFET or MOSDHFET device with 1 $\times$ 150 μm gate dimensions (around 0.25 pF).

The current–voltage characteristics of a single section for the MOSDHFET (150-μm gatewidth) showed the saturation current to be 0.6 A/mm at zero gate bias. It increased to 0.86 A/mm at the positive gate bias of $V_g = +3$ V. The threshold voltage was approximately -9.5 V. The pulsed I–V's show nearly linear scaling with the gate periphery for both device types. However, the dc peak current for both device types saturates when the device periphery exceeds 1.5 mm. The dc current saturation with the increase of the device periphery is due to device self-heating. In pulsed I–V measurements, we achieved the saturation currents as high as 5 A for a 6-mm-wide device [31].

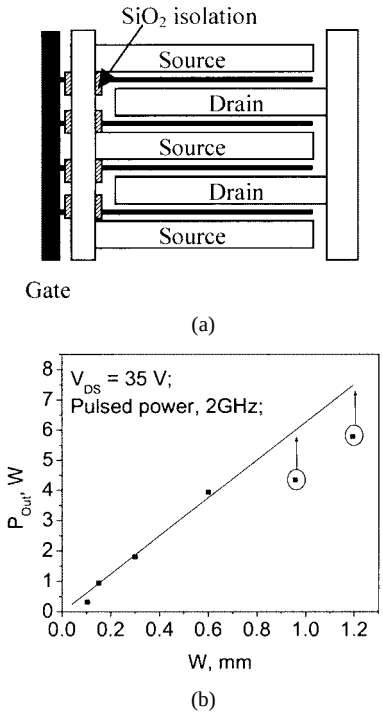


Fig. 9. (a) MG MOSDHFET design and (b) output pulsed power as a function of total gatewidth. Measurements were taken at 35-V pulsed drain bias.

VII. Microwave and Switching Characteristics of MG Insulating Gate Devices

RF testing of MG MOSDHFETs was carried out using an HP 8510C network analyzer for small-signal cutoff- frequency measurements and a Maury Automated Tuner system for large-signal power measurements. The cutoff frequency f_t of 9.5 GHz was measured for a 0.5-mm-wide device with 1-μm gate length at -5-V gate bias. The source– and load–pull high-power measurements were performed at the drain bias of 35 V. This yields the effective saturation velocity

$$v_s = 2\pi L f_t = 0.6\ 10^7 \text{ cm/s}$$

which is in good agreement with the value extracted from the maximum drain saturation current. In Fig. 9, we include the maximum output power as a function of device periphery for the pulse mode testing. The pulse length of 1 μs with the 1% duty cycle was used for these power measurements. Similar to the dc parameters, the RF pulse output powers also scale almost linearly with the device periphery. The output power for the optimally tuned MOSDHFETs is close to 6.3 W/mm. The measured power level was somewhat lower for the narrow device ($W \approx 50$ μm) due to difficulties with tuning to very high input and output impedances. For the largest devices ($W \geq 1$ mm), the available input RF signal was not large enough to saturate the MOSDHFET. Hence, only the power at 3-dB compression was measured and then extrapolated to the saturation level, as shown by vertical arrows in Fig. 9. The MOSDHFET devices demonstrated a very stable behavior under a continuous RF drive. In the course of a 16-h test at 25-V drain bias, the RF power degraded by approximately 0.5–0.6 W/mm in the first 2–3 h of operation and then stabilized. This stabilization was irreversible, i.e., when the test was repeated, the initial

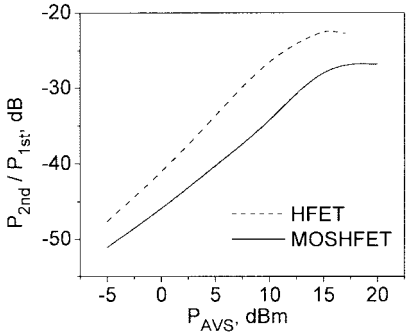


Fig. 10. Comparison of the nonlinear distortion in MOSHFET and HFET devices. The plots show the relative amplitude of the second harmonic of the fundamental frequency of 2 GHz as a function of the input RF power.

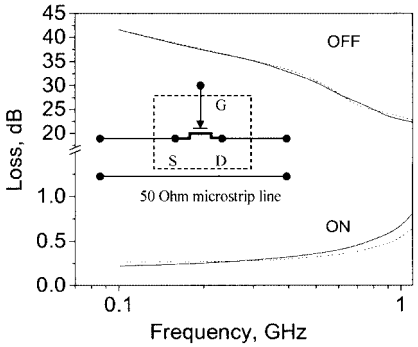


Fig. 11. Test switching circuit based on MG MOSHFET. Solid lines: experimental data for 1 μm $\times$ 1 mm MOSHFET. Dashed lines: simulations.

RF output power was close to its stable value and did not change with time. We believe that this stable MOSDHFET behavior is due to extremely low gate-leakage currents and a perfect confinement of the 2-DEG in the InGaN channel, which avoids trapping and long-term relaxation effects.

The MOSHFET devices have a lower level of nonlinear distortions compared to regular HFETs. This is due to a larger gate-to-channel separation and a more linear transconductance–voltage dependence [7], [8]. In Fig. 10, we show the measured dependencies of the relative level of the second harmonic power on the input RF power for the MOSHFET and HFET fabricated on the same wafer. These measurements were performed at 2-GHz continuous wave (CW) fundamental frequency under 30-V drain bias. As seen, for the MOSHFET, the relative power of the second harmonic is approximately 8 dB lower compared to the HFET.

We have also demonstrated an efficient microwave switch based on an MG AlGaN/GaN MOSHFET. Record high saturation current and breakdown voltage, extremely low gate-leakage current, and low gate capacitance of the MOSHFETs described above make them excellent active elements for RF switching.

The simplest single-element test RF switching circuit is shown in the inset of Fig. 11. In the open state, the MOSHFET switch can be described as a series resistance R connected to the microstrip line with the characteristic impedance Z_0. For $Z_0 = 50\,\Omega$ and $R \ll Z_0$, the insertion loss can be estimated as

$$L_{\rm Ins}\,({\rm dB}) = 10\,{\rm Log}\,\frac{1}{1+R/2Z_0} \approx 0.087 R_{SQ} \times L/W \quad (5)$$

where R_{SQ} is the sheet resistance of the 2-D channel in the source–drain opening of the length L and width W. For a typical MOSHFET with the 5-μm source–drain opening, R_{SQ} $\approx$300–400 Ω at zero gate bias. Since the MOSHFET allows for a high positive gate bias, this resistance can be further decreased by approximately a factor of two. The shunting effect of the gate–source and gate–drain capacitances is insignificant in MOSHFETs due to a larger gate–channel separation and lower gate capacitance. It follows from (5) that the insertion loss of 0.1–0.25 dB can be easily achieved in the ON state for a 1-mm-wide device. For the OFF state, the gate voltage biases the device into the pinchoff state. In this state, the isolation is mainly determined by the source–drain capacitance, assuming that gate is RF grounded. Using a 1-mm-wide MOSHFET with 1-μm-long gate, we have achieved 0.25-dB insertion loss and over 40-dB isolation at 100 MHz (see Fig. 11). The frequency dependence of the insertion loss is mainly due to the series inductance of the bonding wires, as seen from the simulated curve (dashed curve in Fig. 11). The isolation decreases down to 22 dB at 1 GHz due to the drain–source capacitance of 0.01 pF/mm found for the planar device geometry. The maximum MOSHFET switching power in the ON state is limited by the maximum saturation current $I_{\rm DSM}$ and the drain knee voltage $V_{\rm KN}$

$$P_{inm} = \frac{V_{\rm KN} \cdot I_{\rm DSM}}{2}\,\frac{1}{1-K_p}$$

where $K_p = P_{\rm Out}/P_{\rm In}$ is the power transfer ratio of the switch. As shown above, both these parameters are higher for the MOSHFETs compared to the HFETs. Using $I_{\rm DSM} \approx 1.6$ A/mm and $V_{\rm KN} \approx 5$ V and $K_p \approx 0.95$ (corresponding to 0.2-dB insertion loss), the maximum switching power of the MOSHFET-based switch can be estimated as $P_{inm} = 80$ W/mm. This power level is approximately 80 times higher than that reported for a GaAs-based switch [32]. These results show a high potential of MOSHFET devices for microwave switching. As we have shown before [33], the MOSHFETs can also be used as extremely high-power dc switching devices. The breakdown voltage as high as 500 V was measured for the MOSHFET devices with the 10-μm gate-to-drain opening. With the maximum current of the MOSHFET of approximately 5 A (as demonstrated above for the 6-mm-wide device), the maximum switching power was 7.5 kW/mm^2. For these estimations, we used the total device area including a 100-μm separation between the adjacent gate sections. If only the active source–drain region area is used for this estimate, the switched power density estimate increases to 50 kW/mm^2.

VIII. Conclusions

The insulating gate III-N devices demonstrate a much superior performance compared to regular AlGaN/GaN HFETs. The gate-leakage current for these devices is 4–6 orders of magnitude lower; the maximum saturation currents might be twice as high. The combination of the MOS design with a double-heterostructure transistor design, i.e., the DHFET, results in a low gate-leakage current collapse-free MOSDHFET device. Due to a larger threshold voltage and gate voltage swing,

the MOSHFETs and MOSDHFETs have a lower level of RF nonlinear distortions. They can be used as extremely efficient microwave and power switches.

REFERENCES

[1] M. A. Khan, J. M. Van Hove, J. N. Kuznia, and D. T. Olsen, "High electron mobility GaN–AlGaN heterostructures grown by LPMOCVD," *Appl. Phys. Lett.*, vol. 58, p. 2408, 1991.

[2] M. A. Khan, J. N. Kuznia, J. M. Van Hove, N. Pan, and N. Carter, "Observation of a two-dimensional electron gas in low pressure MOCVD deposited GaN/AlGaN heterojunctions," *Appl. Phys. Lett.*, vol. 60, p. 3027, 1992.

[3] T. Sheppard, W. L. Pribble, D. T. Emerson, Z. Ring, R. P. Smith, S. T. Allen, and J. W. Palmour, "High power demonstration at 10 GHz with FaN/A1GaN HEMT hybrid amplifier," in *Device Research Conf. Dig.*, 2000, p. 37.

[4] N. X. Nguyen, M. Micovic, W.-S. Wong, P. Hashimoto, L.-M. McCray, P. Janke, and C. Nguyen, "High performance microwave power GaN/A1GaN MODFETs gron by RF-assisted MBE," *Electron. Lett.*, vol. 36, p. 468, 2000.

[5] Y.-F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, pp. 586–590, Mar. 2001.

[6] W. Lu, J. Yang, M. A. Khan, and I. Adesida, "AlGaN/GaN HEMT's on SiC with over 100 GHz fT and low microwave noise," *IEEE Trans. Electron Devices*, vol. 48, pp. 581–585, Mar. 2001.

[7] M. A. Khan, X. Hu, G. Simin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, "AlGaN/GaN metal–oxide–semiconductor heterostructure field effect transistor," *IEEE Electron Device Lett.*, vol. 21, pp. 63–65, Feb. 2000.

[8] M. A. Khan, X. Hu, G. Simin, J. Yang, R. Gaska, and M. S. Shur, "AlGaN/GaN metal–oxide–semiconductor heterostructure field effect transistors on SiC substrates," *Appl. Phys. Lett.*, vol. 77, pp. 1339–1341, 2000.

[9] M. A. Khan, J. W. Yang, G. Simin, H. zur Loye, R. Bicknell-Tassius, R. Gaska, M. S. Shur, G. Tamulaitis, and A. Žukauskas, "Energy band/lattice mismatch engineering in quaternary AlInGaN/GaN heterostructure," *Phys. Status Solidi (a)*, vol. 176, no. 1, pp. 227–230, 1999.

[10] J. B. Webb, H. Tang, S. Rolfe, and J. A. Baedwell, "Semi-insulating C-doped GaN and high-mobility AlGaN/GaN heterostructures grown by ammonia molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 75, no. 7, pp. 953–955, 1999.

[11] G. Simin, A. Tarakji, X. Hu, A. Koudymov, J. Yang, M. A. Khan, M. S. Shur, and R. Gaska, "High-temperature performance of AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect-transistors," *Phys. Status Solidi (a)*, pt. 1, vol. 188, pp. 219–222, 2001.

[12] A. Koudymov, G. Simin, J. Yang, M. A. Khan, A. Tarakji, X. Hu, M. S. Shur, and R. Gaska, "Maximum current in nitride based heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 80, pp. 3216–3218, 2002.

[13] M. S. Shur, *GaAs Devices and Circuits*. New York: Plenum, 1987.

[14] M. S. Shur, A. D. Bykhovski, and R. Gaska, "Two dimensional hole gas induced by piezoelectric and pyroelectric charges," *Solid State Electron. (Special Issue)*, vol. 44, pp. 205–210, 2000.

[15] F. Ren, M. Hong, S. N. G. Chu, M. A. Marcus, M. J. Schurman, A. Baca, S. J. Pearton, and C. R. Abernathy, "Effect of temperature on Ga_2O_3 (Gd_2O_3)/GaN metal oxide semiconductor field effect transistor," *Appl. Phys. Lett.*, vol. 73, p. 3893, 1998.

[16] M. S. Shur and M. A. Khan, "Optoelectronic GaN-based field effect transistors," in *Proc. SPIE Optoelectronic Materials, Devices, and Integrated Circuits*, Feb. 7, 1995, Paper 2397, pp. 294–303.

[17] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics on undoped A1GaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, pp. 268–270, June 2000.

[18] L. F. Eastman, V. Tilak, J. Smart, B. M. Green, E. M. Chumbes, R. Dimitrov, H. Kim, O. S. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. J. Schaff, and J. R. Shealy, "Undoped AlGaN/GaN HEMT's for microwave power amplification," *IEEE Trans. Electron Devices*, vol. 48, pp. 479–485, Mar. 2001.

[19] X. Hu, A. Koudymov, G. Simin, J. Yang, M. A. Khan, A. Tarakji, M. S. Shur, and R. Gaska, "Si_3N_4/AlGaN/GaN–metal–insulator-semiconductor heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 79, pp. 2832–2834, 2001.

[20] A. Tarakji, G. Simin, N. Ilinskaya, X. Hu, A. Kumar, A. Koudymov, J. Zhang, M. A. Khan, M. S. Shur, and R. Gaska, "Mechanism of radio-frequency current collapse in GaN–A1GaN field-effect transistors," *Appl. Phys. Lett.*, vol. 78, pp. 2169–2171, 2001.

[21] C. Nguyen, N. X. Nguyen, and D. E. Grider, "Drain current compressoin in GaN MODFETs under large-signal modulation at microwave frequencies," *Electron. Lett.*, vol. 35, pp. 1380–1382, 1999.

[22] E. Kohn, I. Daumiller, P. Schmid, N. X. Nguyen, and C. N. Nguyen, "Large signal frequency dispersion of A1GaN/GaN heterostructure field effect transistors," *Electron. Lett.*, vol. 35, pp. 1022–1024, 1999.

[23] R. Dietrich, A. Wieszt, A. Vescan, H. Leier, J. M. Redwing, K. S. Boutros, K. Kornitzer, R. Freitag, T. Ebner, and K. Thonke, "Current limitation after pinch-off in A1GaN/GaN FETs," *MRS Internet J. Nitride Semiconduct. Res.*, vol. 5, no. 2, pp. 1–4, 2000.

[24] P. B. Klein, S. C. Binari, J. A. Freitas, Jr., and A. E. Wickenden, "Photoionization spectroscopy of traps in GaN metal–semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 88, pp. 2843–2852, 2000.

[25] I. Daumiller, D. Theron, C. Gaquiere, A. Vescan, R. Dietrikh, A. Wieszt, H. Leier, B. Vetury, U. K. Mishra, I. P. Smorchkova, S. Keller, N. X. Nguyen, C. Nguyen, and E. Kohn, "Current instabilities in GaN-base devices," *IEEE Electron Device Lett.*, vol. 22, pp. 62–64, Feb. 2001.

[26] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped A1Gan/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, pp. 268–270, June 2000.

[27] G. Simin, A. Koudymov, A. Tarakji, X. Hu, J. Yang, M. A. Khan, M. S. Shur, and R. Gaska, "Induced strain mechanism of current collapse in AlGaN/GaN heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 79, pp. 2651–2653, 2001.

[28] S. M. Baier, N. C. Cirillo, Jr., S. A. Hanka, and M. S. Shur, "Gated transmission line model structure for characterization of FETs," U.S. Patent 4 638 341, Jan. 20, 1987.

[29] G. Simin, X. Hu, A. Tarakji, J. Zhang, A. Koudymov, S. Saygi, J. Yang, M. A. Khan, M. Shur, and R. Gaska, "AlGaN/InGaN/GaN double heterostructure field-effect transistor," *Jpn. J. Appl. Phys.*, vol. 40, no. 11A, pp. L1142–L1144, 2002.

[30] G. Simin, A. Koudymov, H. Fatima, J. Zhang, J. Yang, M. A. Khan, X. Hu, A. Tarakji, R. Gaska, and M. S. Shur, "SiO_2/AlGaN/InGaN/GaN MOSDHFETs," *IEEE Electron Device Lett.*, vol. 23, pp. 458–460, Aug. 2002.

[31] G. Simin, X. Hu, N. Ilinskaya, J. Zhang, A. Tarakji, A. Kumar, M. A. Khan, R. Gaska, and M. S. Shur, "Large periphery high-power AlGaN/GaN metal–oxide–semiconductor heterostructure field effect transistors on SiC with oxide-bridging," *IEEE Electron Device Lett.*, vol. 22, no. 2, pp. 53–55, 2001.

[32] A. Gopinath and J. B. Rankin, "GaAs FET RF switches," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1272–1278, 1985.

[33] G. Simin, X. Hu, N. Ilinskaya, A. Kumar, A. Koudymov, J. Zhang, M. A. Khan, R. Gaska, and M. S. Shur, "A 7.5 kW/mm^2 current switch using AlGaN/GaN metal–oxide–semiconductor heterostructure field effect transistors on SiC substrates," *Electron. Lett.*, vol. 36, pp. 2043–2044, Nov. 2000.

M. Asif Khan (SM'02) received the Ph.D. degree from the Massachusetts Institute of Technology, Cambridge, in 1979.

He then joined the University of South Carolina, Raleigh, to head up the new Microelectronics Laboratory. The initial focus of the program is on the fabrication of AlGaN- and SiC-based high-power microwave transistors for high-temperature operations. He was previously Vice President, Optoelectronics, for APA Optics Inc., Blaine, MN, where his research group performed the pioneering work in the development of GaN–AlGaN materials and devices. Prior to that, he was the Principal Scientist of research and development groups at 3M and Honeywell Inc. He has authored over 150 refereed papers, several book chapters, and over 25 invited papers.

Grigory Simin (A'01–M'01) received the M.S.S.E. degree from the Leningrad Electrotechnical Institute, Leningrad, Russia, in 1971, the Ph.D. degree in physics (physics of semiconductors and dielectrics) from the GIRICOND Science and Research Institute, Leningrad, Russia, in 1979, and Senior Research Scientist Diploma from the Supreme State Committee on Academic Degrees, St. Petersburg, Russia, in 1985.

Since 1998, he has been with the Department of Electrical Engineering, University of South Carolina, where he has been a Research Professor and, since 2001, an Associate Professor. His research focus is GaN-based electronic and opto-electronic devices. He has authored four books, several book chapters on the physics of semiconductor devices, and over 100 papers in referred journals. His research has included Gunn-effect devices, GaAs MESFETs, microwave and optical integrated circuits, and semiconductor lasers.

Jinwei Yang received the Ph.D. degree in materials science and engineering from Case Western Reserve University, Cleveland, OH, in 1993.

He was a Senior Research Scientist with APA Optics Inc. Since 1997, he has been a Research Professor of electrical engineering with the University of South Carolina, Raleigh. His areas of research interest include MOCVD growth of III-N materials, sublimation growth of bulk SiC, TEM, HRTEM, and X-ray diffraction analysis of crystal defects in electronic materials.

Jianping Zhang received the Ph.D. degree from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, in 1999.

His research has focused on MBE and MOCVD III-N growth and characterization. He is currently focused on MOCVD AlInGaN materials growth for deep UV emitters.

Alexei Koudymov received the M.D. degree from the St.-Petersburg State Technical University, St.-Petersburg, Russia, in 1997.

He specializes in GaN-based devices characterization.

Michael S. Shur (M'79–SM'83–F'89) received the M.S.E.E. degree (with honors) from St.-Petersburg Electrotechnical Institute, St.-Petersburg, Russia, in 1965, Ph.D. degree in physics and mathematics from the A. F. Ioffe Institute of Physics and Technology, St. Petersburg, Russia, in 1967.

He has held research or faculty positions with different universities including the A. F. Ioffe Institute, Cornell University, University of Minnesota, and University of Virginia, where he was the John Money Professor of Electrical Engineering and served as Director of the Applied Electrophysics Laboratories. He is currently Patricia W. and C. Sheldon Roberts'48 Professor of Solid State Electronics, Professor of Physics, Applied Physics and Astronomy, Professor of Information Technology, and Associate Director of Center for Integrated Electronics and Electronics Manufacturing with the Rensselaer Polytechnic Institute (RPI), Troy, NY. He is Editor-in-Chief of the *International Journal of High Speed Electronics and Systems*. He is Editor of a book series on special topics in electronics and systems published by World Scientific. He is a member of the Honorary Board of *Solid State Electronics*. He is a co-developer of AIM-Spice. In 2000, he was listed as one of the most quoted researchers in his field.

Remis Gaska received the Ph.D. degree in physics from Vilnius University, Vilnius, Lithuania, in 1988, and Ph.D. degree in electrical engineering from Wayne State University, Detroit, MI, in 1996.

Prior to starting Sensor Electronics Technology Inc., Columbia, SC, he was the Research and Development Program Manager at APA Optics, Minneapolis, MN, and Research Associate Professor with Rensselaer Polytechnic Institute, Troy, NY. His group developed AlGaN/GaN-based advanced electronic and opto-electronic devices, which include GaN and AlGaN ultraviolet Schottky photodetectors and p-n photodiodes, high-power AlGaN/GaN HFETs, and piezoelectric sensors. His III–V nitride research results were published in over 200 technical papers and conference presentations.

Xuhong Hu (M'01) received the Ph.D. degree in electrical engineering from the University of South Carolina, Raleigh, in 2001.

His research interest includes device design, fabrication, and characterization of high-power AlGaN/GaN MOSHFETs. He fabricated the novel AlGaN/GaN MOSHFET device with a thin SiO_2 film as the gate insulator. In May 2001, he joined Sensor Electronic Technology Inc., Columbia, SC, where he is involved with GaN-based electronic device design, fabrication, and characterization. He has authored or coauthored over 20 papers in refereed journals.

Ahmad Tarakji is currently working toward the Ph.D. degree in electrical engineering from the University of South Carolina, Raleigh.

Since March 2001, he has been with Sensor Electronic Technology Inc., Columbia, SC, where he has been involved with microwaves evaluations of GaN-based electronic devices. He is the principal author and coauthor of over 20 journal papers in areas as diverse as semiconductor devices, analog very large scale integration (VLSI), digital filtering, and power systems. His current research interests are focused on the high-frequency characterization and reliability evaluation of microwave devices based on wide-bandgap materials, design optimizations for the high-power high-frequency III-N devices, and modeling of heterostructure devices. He has also made over a dozen conference presentations.